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1 Breakpoints and breakpoint detection in source-level emulation
Gernot H. Koch, W. Rosenstiel, U. Kebschull
April 1998 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 3 Issue 2
Publisher: ACM Request Permissions
Full text available: Pdf (203.65 KB) Additional Information: full citation, abstract, references, index terms
Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 16, Downloads (Overall): 212, Citation Count: 1

We present an approach for accelerating the validation speed of behavioral system descriptions through hardware emulation. The method allows source-level debuggingof running hardware specified in behavioral VH DL in a way similar to sorce-leve debugging ...

Keywords: debugging, emulation, high-level synthesis

2 A reconfigurable hardware approach to network simulation
Dimitrios Stiliadis, Anujan Varma
January 1997 **Transactions on Modeling and Computer Simulation (TOMACS)** , Volume 7 Issue 1
Publisher: ACM Request Permissions
Full text available: Pdf (925.18 KB) Additional Information: full citation, references, cited by, index terms, review
Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 20, Downloads (Overall): 435, Citation Count: 2

Keywords: ATM switch scheduling, field-programmable gate array, hardware simulation

3 Reconfigurable computing: a survey of systems and software
Katherine Compton, Scott Hauck
June 2002 **Computing Surveys (CSUR)** , Volume 34 Issue 2
Publisher: ACM Request Permissions
Full text available: Pdf (710.56 KB) Additional Information: full citation, abstract, references, cited by, index terms, review
Bibliometrics: Downloads (6 Weeks): 96, Downloads (12 Months): 851, Downloads (Overall): 7453, Citation Count: 11

Due to its potential to greatly accelerate a wide variety of applications, reconfigurable computing has become a subject of a great deal of research. Its key feature is the ability to perform computations in hardware to increase performance, while retaining ...

Keywords: Automatic design, FPGA, field-programmable, manual design, reconfigurable architectures, reconfigurable computing, reconfigurable systems

4 A software development tool chain for a reconfigurable processor
Alberto La Rosa, Luciano Lavagno, Claudio Passerone
November 2001 **CASES '01:** Proceedings of the 2001 international conference on Compilers, architecture, and synthesis for embedded systems
Publisher: ACM
Full text available: Pdf (79.88 KB) Additional Information: full citation, references, cited by, index terms
Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 38, Downloads (Overall): 503, Citation Count: 7

5 A reconfigurable logic machine for fast event-driven simulation
Jerry Bauer, Michael Bershteyn, Ian Kaplan, Paul Vyedin
May 1998 **DAC '98:** Proceedings of the 35th annual Design Automation Conference
Publisher: ACM Request Permissions
Full text available: Pdf (129.52 KB) Additional Information: full citation, abstract, references, cited by, index terms
Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 25, Downloads (Overall): 242, Citation Count: 9

As the density of VLSI circuits increases, software techniques cannot effectively simulate designs through the millions of simulation cycles needed for verification. Emulation can supply the necessary capacity and

performance, but emulation is limited ...

Keywords: event-driven simulation, reconfigurable computing

6 Recent developments in high-level synthesis
Youn-Long Lin
January 1997 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 2 Issue 1
Publisher: ACM Request Permissions
Full text available: Pdf (232.47 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 91, Downloads (Overall): 2253, Citation Count: 16

We survey recent developments in high level synthesis technology for VLSI design. The need for higher-level design automation tools are discussed first. We then describe some basic techniques for various subtasks of high-level synthesis. Techniques that ...

Keywords: VLSI design, design automation, design methodology, high level synthesis

7 Using rapid prototyping in computer architecture design laboratories
James O. Hamblen, Henry Owen, Sudhakar Yalamanchili, Binh Dao
January 1996 **WCAE-2 '96:** Proceedings of the 1996 workshop on Computer architecture education
Publisher: ACM
Full text available: Pdf (243.40 KB) Additional Information: full citation, abstract, references

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 20, Downloads (Overall): 104, Citation Count: 3

This paper describes the undergraduate computer architecture courses and laboratories introduced at Georgia Tech during the past two years. A core sequence of six required courses for computer engineering students has been developed. In this paper, emphasis ...

8 High-level modeling and FPGA prototyping of microprocessors
Joydeep Ray, James C. Hoe
February 2003 **FPGA '03:** Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays
Publisher: ACM Request Permissions
Full text available: Pdf (148.95 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 31, Downloads (Overall): 603, Citation Count: 4

Emerging high-level hardware description and synthesis technologies in conjunction with field-programmable gate arrays (FPGAs) have significantly lowered the threshold for hardware development. Opportunities exist to integrate these technologies into ...

Keywords: FPGA, evaluation, microarchitecture, microprocessor, operation-centric, prototyping

9 Functional verification methodology of Chameleon processor
Francoise Casaubieilh, Anthony Mclsaac, Mike Benjamin, Mike Bartley, Francois Pogodalla, Frédéric Pecheteau, Mohamed Belhadi, Jeremy Eggleton, Gérard Mas, Geoff Barrett, Christian Berthet
June 1996 **DAC '96:** Proceedings of the 33rd annual Design Automation Conference
Publisher: ACM Request Permissions
Full text available: Pdf (62.38 KB) Additional Information: full citation, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 14, Downloads (Overall): 273, Citation Count: 14

10 Instruction Set Emulation for Rapid Prototyping of SoCs
Jurgen Schnerr, Gunter Haug, Wolfgang Rosenstiel
March 2003 **DATE '03: Proceedings of the conference on Design, Automation and Test in Europe - Volume 1** , Volume 1
Publisher: IEEE Computer Society
Full text available: Pdf (129.16 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 10, Downloads (Overall): 99, Citation Count: 2

In this paper the application of Instruction Set Emulation for rapid prototyping of SoCs will be presented. The emulation works in a way that both the software and the hardware behaviour of the emulated processor core is reproduced cycle accurately. ...

11 A hierarchical approach for energy efficient application design using heterogeneous embedded systems
Sumit Mohanty, Viktor K. Prasanna
October 2003 **CASES '03:** Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems
Publisher: ACM
Full text available: Pdf (399.12 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 35, Downloads (Overall): 562, Citation Count: 1

Several features such as reconfiguration, voltage and frequency scaling, low-power operating states, duty-cycling, etc. are exploited for latency and energy efficient application design using heterogeneous embedded systems. However, more choices during ...

Keywords: design space exploration, energy efficiency, heterogeneous embedded systems, performance estimation

12 A hardware/software co-design flow and IP library based on simulink
L. M. Reyneri, F. Cucinotta, A. Serra, L. Lavagno
June 2001 **DAC '01:** Proceedings of the 38th annual Design Automation Conference
Publisher: ACM Request Permissions
Full text available: Pdf (119.94 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 53, Downloads (Overall): 480, Citation Count: 4

This paper describes a design flow for data-dominated embedded systems. We use The Mathworks' Simulink\trademark environment for functional specification and algorithmic analysis. We developed a library of Simulink blocks, each parameterized by design ...

13 TIERS: Topology independent pipelined routing and scheduling for VirtualWire compilation
Charles Selvidge, Anant Agarwal, Matt Dahl, Jonathan Babb
February 1995 **FPGA '95:** Proceedings of the 1995 ACM third international symposium on Field-programmable gate arrays
Publisher: ACM Request Permissions
Full text available: Pdf (180.92 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 18, Downloads (Overall): 187, Citation Count: 6

TIERS is a new pipelined routing and scheduling algorithm implemented in a complete VirtualWireTM compilation and synthesis system. TIERS is described and compared to prior work both analytically and quantitatively. TIERS improves ...

14 Hardware-assisted simulated annealing with application for fast FPGA placement
Michael G. Wrighton, André M. DeHon
February 2003 **FPGA '03:** Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays
Publisher: ACM Request Permissions
Full text available: Pdf (503.33 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 25, Downloads (Overall): 590, Citation Count: 7

To truly exploit FPGAs for rapid turn-around development and prototyping, placement times must be reduced to seconds; late-bound, reconfigurable computing applications may demand placement times as short as microseconds. In this paper, we show how a ...

Keywords: design automation, field-programmable gate arrays, placement, reconfigurable computing, simulated annealing

15 An approach for integrated specification and design of real-time systems
Y. Tanurhan, H. Götz, S. Schmerler, K. Müller-Glaser
September 1996 **EURO-DAC '96/ EURO-VHDL '96:** Proceedings of the conference on European design automation
Publisher: IEEE Computer Society Press
Full text available: Pdf (68.59 KB) Additional Information: full citation, references, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 15, Downloads (Overall): 377, Citation Count: 0

16 Functional partitioning improvements over structural partitioning for packaging constraints and synthesis: tool performance
Frank Vahid, Thuy Dm Le, Yu-Chin Hsu
April 1998 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 3 Issue 2
Publisher: ACM Request Permissions
Full text available: Pdf (225.74 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 34, Downloads (Overall): 328, Citation Count: 5

Incorporating functional partitioning into a synthesis methodology leads to several important advantages. In functional partitioning, we first partition a functional specification into smaller subspecifications and then synthesize structure for each, ...

Keywords: behavioral synthesis, functional partitioning, system-level design

17 Automatic Evaluation of the Accuracy of Fixed-Point Algorithms
D. Menard, O. Sentieys
March 2002 **DATE '02:** Proceedings of the conference on Design, automation and test in Europe
Publisher: IEEE Computer Society
Full text available: Pdf (263.13 KB) Additional Information: full citation, abstract, cited by

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 26, Downloads (Overall): 236, Citation Count: 7

The minimization of cost, power consumption and time-to-market of DSP applications requires the developmentof methodologies for the automatic implementation offloating-point algorithms in fixed-point architectures. Inthis paper, a new methodology for ...

18 Wormhole IP over (connectionless) ATM
Manolis G. H. Katevenis, Iakovos Mavroidis, Georgios Sapountzis, Eva Kalyvianaki, Ioannis Mavroidis, Georgios Glykopoulos
October 2001 **IEEE/ ACM Transactions on Networking (TON)** , Volume 9 Issue 5
Publisher: IEEE Press
Full text available: Pdf (211.25 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 21, Downloads (Overall): 346, Citation Count: 1

High-speed switches and routers internally operate using fixed-size cells or segments; variable-size packets are segmented and later reassembled. Connectionless ATM was proposed to quickly carry IP packets segmented into cells (AAL5) using a number of ...

Keywords: Connectionless ATM, IP over ATM, gigabit router, routing filter, wormhole IP, wormhole routing

19 Data memory minimisation for synchronous data flow graphs emulated on DSP-FPGA targets
Marleen Adé, Rudy Lauwereins, J. A. Peperstraete
June 1997 **DAC '97:** Proceedings of the 34th annual Design Automation Conference
Publisher: ACM Request Permissions
Full text available: Pdf (278.40 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 33, Downloads (Overall): 191, Citation Count: 11

The paper presents an algorithm to determine the close-to-smallestpossible data buffer sizes for arbitrary synchronous dataflow (SDF) applications, such that we can guarantee the existenceof a deadlock free schedule. The presented algorithm fits inthe ...

20 Energy/power estimation of regular processor arrays
Steven Derrien, Sanjay Rajopadhye
October 2002 **ISSS '02:** Proceedings of the 15th international symposium on System Synthesis
Publisher: ACM
Full text available: Pdf (909.01 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 9, Downloads (Overall): 167, Citation Count: 0

We propose a high-level analytical model for estimating the energy and/or power dissipation in VLSI processo (systolic) array implementations of loop programs, particularly for implementations on FPGA based CO-processors. We focus on the respective ...

Keywords: design space exploration, power estimation, processor array partitioning, programmable logic

Result page: **1** 2 next >>